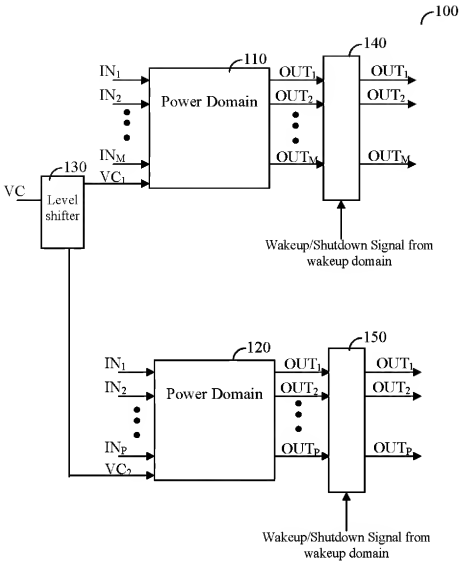


FIGURE 1 (PRIOR ART)

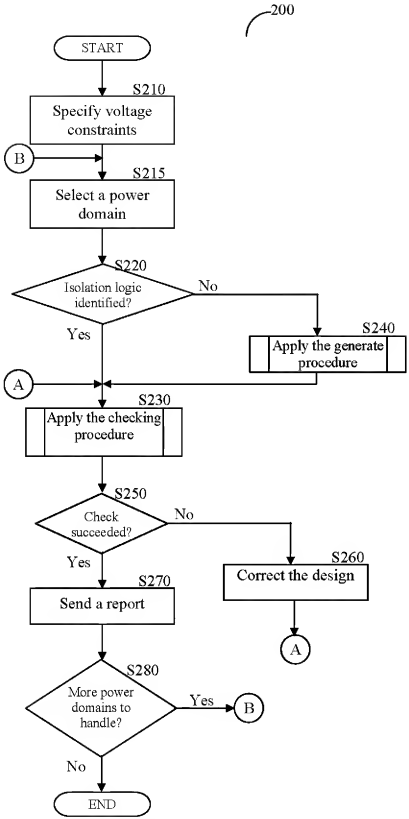

200
START
S210
Specify voltage constraints
B
S215
Select a power domain
S220
Isolation logic identified?
No
Yes
S240
Apply the generate procedure
A
S230
Apply the checking procedure
S250
Check succeeded?
No
Yes
S260
Correct the design
S270
Send a report
A
S280
More power domains to handle?
Yes
B
No
END

FIGURE 2

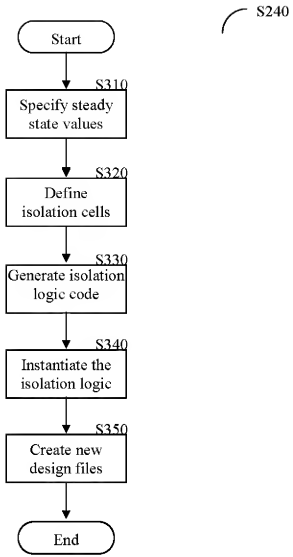

S240
Start
S310
Specify steady state values
S320
Define isolation cells
S330
Generate isolation logic code
S340
Instantiate the isolation logic
S350
Create new design files
End

FIGURE 3

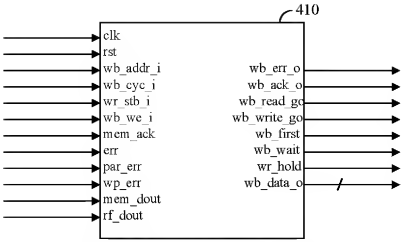
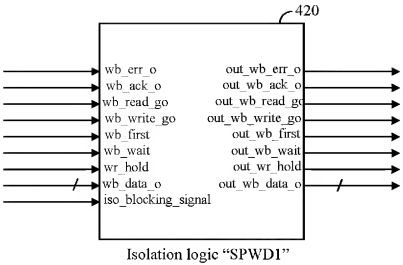

410
clk
rst
wb_addr_i
wb_cyc_i
wr_stb_i
wb_we_i
mem_ack
err
par_err
wp_err
mem_dout
rf_dout
wb_err_o
wb_ack_o
wb_read_go
wb_write_go
wb_first
wb_wait
wr_hold
wb_data_o
Memory Controller (mc_top) for SPWD1

FIGURE 4A

```
4000    module
        iso_logic_block_for_SPDW1_1(out_wb_data_o,out_wb_ack_o,out_wb_err_o,out_wb_
        read_go,out_wb_write_go,out_wb_first,out_wb_wait,out_wr_hold,wb_data_o,wb_ack_
        o,wb_err_o,wb_read_go,wb_write_go,wb_first,wb_wait,wr_hold,iso_signal_blocking);

4010    input [31:0] wb_data_o ;
4020    input wb_ack_o ;
4030    input wb_err_o ;
4040    input wb_read_go ;
4050    input wb_write_go ;
4060    input wb_first ;
4080    input wb_wait ;
4090    input wr_hold ;
4100    input iso_signal_blocking ;

4110    output [31:0] out_wb_data_o ;
4120    output out_wb_ack_o ;
4130    output out_wb_err_o ;
4140    output out_wb_read_go ;
4150    output out_wb_write_go ;
4160    output out_wb_first ;
4170    output out_wb_wait ;
4170    output out_wr_hold ;

4180    wire iso_signal_blocking_n;

4190    assign iso_signal_blocking_n = ~iso_signal_blocking;
4200    assign out_wr_hold = iso_signal_blocking_n & wr_hold;
4210    assign out_wb_wait = iso_signal_blocking | wb_wait;
4220    assign out_wb_first = iso_signal_blocking | wb_first;
4230    assign out_wb_write_go = iso_signal_blocking_n & wb_write_go;
4240    assign out_wb_read_go = iso_signal_blocking_n & wb_read_go;
4250    assign out_wb_err_o = iso_signal_blocking_n & wb_err_o;
4260    assign out_wb_ack_o = iso_signal_blocking | wb_ack_o;
4270    assign out_wb_data_o[31] = iso_signal_blocking_n & wb_data_o[31];
4280    assign out_wb_data_o[30] = iso_signal_blocking_n & wb_data_o[30];
.
.
.
4560    assign out_wb_data_o[2] = iso_signal_blocking_n & wb_data_o[2];
4570    assign out_wb_data_o[1] = iso_signal_blocking_n & wb_data_o[1];
4580    assign out_wb_data_o[0] = iso_signal_blocking_n & wb_data_o[0];

4590    endmodule
```

FIGURE 4B



Isolation logic "SPWD1"

FIGURE 4C

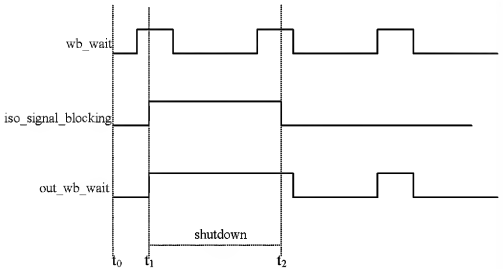


FIGURE 4D

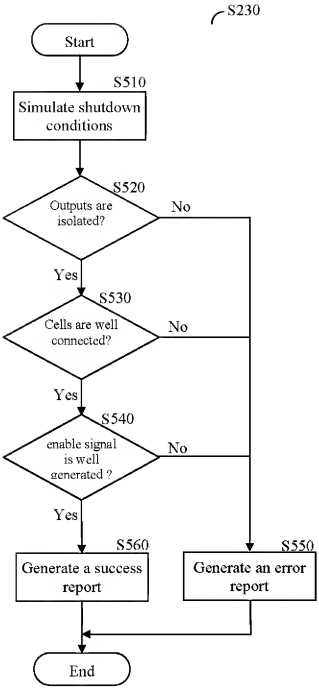

S230
Start
S510
Simulate shutdown conditions
S520
Outputs are isolated?
No
Yes
S530
Cells are well connected?
No
Yes
S540
enable signal is well generated ?
No
Yes
S560
Generate a success report
S550
Generate an error report
End

FIGURE 5

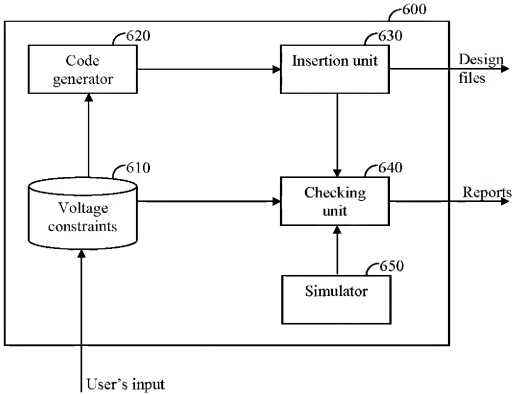

600
620
Code generator
630
Insertion unit
Design files
610
Voltage constraints
640
Checking unit
Reports
650
Simulator
User's input

FIGURE 6